1	Application No.	Applicant(s)	
	10/735,171	AN ET AL.	
Notice of Allowability	Examiner	Art Unit	
	H.Jey Tsai	2812	An
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.			
1. This communication is responsive to			
2. The allowed claim(s) is/are 6.			
3. \boxtimes The drawings filed on <u>12 December 2003</u> are accepted by	the Examiner.		
 4.			
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date	5. ☐ Notice of Informal P 6. ☐ Interview Summary Paper No./Mail Dat 7. ☐ Examiner's Amendn 8. ☑ Examiner's Stateme 9. ☐ Other	(PTO-413), te nent/Comment	

Art Unit: 2812

Reasons For Allowance

The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The basis for the allowability is:

Prior art of record does not teach forming a device wafer by forming a lower silicon on a lower glass substrate; etching the lower silicon for forming a side movement sensing structure including a structure being movable in a horizontal direction on the lower silicon and an sensing electrode for sensing a variation of a capacity as the structure horizontally moves, a first fixed point, and a first border for bonding, etching the lower glass substrate as a sacrificial layer, separately evaporating Au for bonding on the lower silicon layer, forming a cap wafer by forming an upper silicon on an upper glass substrate, forming a gap in the upper silicon, forming an second fixed point, an second border and a second sensing electrode, which correspond to the first fixed point, the first border and the structure movable in a horizontal direction in the device wafer process, forming the via hole from an upper glass substrate to the second fixed point, bonding the device wafer and the cap wafer by a eutectic bonding, evaporating an electric conduction layer on the via hole to form an electric conduction wiring.

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably **accompany** the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the customer service whose telephone number is (703) 308-4357.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679.

The fax phone number for this Group is (703) 872-9306.

hjt

8/31/04

H. Jey Tsai Primary Examiner Patent Examining Group 2800